IN THE CLAIMS

Please amend claims 1, 12, and 16 as indicated below. No amendments are made to the other claims.

1. (Currently Amended) An interposer to couple a die to a substrate and comprising:

a plurality of power and ground vias in a core region of the interposer;

a plurality of signal vias in a peripheral region of the interposer;

an embedded capacitor having first and second terminals;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias; and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die through controlled collapse chip connect solder bumps;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

2. (Previously Presented) The interposer recited in claim 1 wherein the second plurality of power lands and the second plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the substrate.

3-5. (Canceled)

6. (Original) The interposer recited in claim 1 wherein the capacitor comprises at least one high permittivity layer.

7. (Original) The interposer recited in claim 1 wherein the capacitor comprises a plurality of high permittivity layers.

8. (Previously Presented) The interposer recited in claim 7 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals, respectively.

9-11. (Canceled)

12. (Currently Amended) An electronic assembly comprising:

a die comprising a first plurality of power nodes and a first plurality of ground nodes;

a substrate comprising a second plurality of power nodes and a second plurality of ground nodes; and

an interposer coupling the die to the substrate and including

a plurality of power and ground vias in a core region of the interposer;

a plurality of signal vias in a peripheral region of the interposer;

an embedded capacitor having a first terminal and a second terminal;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias; and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground ~~mound~~ lands coupled to the second terminal through second ones of the plurality of ground ~~mound~~ vias;

wherein the first plurality of power lands and the first plurality of ground lands are coupled to the respective first plurality of power nodes and first plurality of ground nodes of the die;

wherein the second plurality of power lands and the second plurality of ground lands are coupled to the respective second plurality of power nodes and second plurality of ground nodes of the substrate;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

13. (Original) The electronic assembly recited in claim 12 wherein the capacitor comprises a plurality of high permittivity layers.

14. (Previously Presented) The electronic assembly recited in claim 13 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals, respectively.

15. (Canceled)

16. (Currently Amended) An electronic system comprising an electronic assembly comprising:

a die comprising a first plurality of power nodes and a first plurality of ground nodes;

a substrate comprising a second plurality of power nodes and a second plurality of ground nodes;[,] and

an interposer coupling the die to the substrate and including

a plurality of power and ground vias in a core region of the interposer;

a plurality of signal vias in a peripheral region of the interposer;

an embedded capacitor having a first terminal and a second terminal;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground ~~around~~ lands coupled to the second terminal through first ones of the plurality of ground vias;[,] and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are coupled to the respective first plurality of power nodes and first plurality of ground ~~mound~~ nodes of the die;[: and]

wherein the second plurality of power lands and the second plurality of ground lands are coupled to the respective second plurality of power nodes and second plurality of ground nodes of the substrate;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

17. (Original) The electronic system recited in claim 16 wherein the capacitor comprises a plurality of high permittivity layers.

18. (Previously Presented) The electronic system recited in claim 17 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals, respectively.

19-31. (Canceled)

32. (Previously Presented) The interposer recited in claim 1, wherein the interposer comprises a multilayer ceramic structure.

33. (Previously Presented) The interposer recited in claim 1, wherein at least one of the power vias does not go entirely through the interposer.

34. (Previously Presented) The interposer recited in claim 1, wherein at least one of the ground vias does not go entirely through the interposer.

35. (Previously Presented) The interposer recited in claim 1, wherein the plurality of power and ground vias is a relatively large number.

36. (Previously Presented) An interposer to couple a die to a substrate and comprising:

a plurality of power and ground vias in a core region of the interposer;

a plurality of signal vias in a peripheral region of the interposer;

an embedded capacitor having a first terminal and a second terminal;

a first surface including a first plurality of power lands coupled to the first terminal through the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through the plurality of ground vias; and

a second surface including a second plurality of power lands coupled to the first terminal through the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die through controlled collapse chip connect solder bumps;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

37. (Previously Presented) The interposer recited in claim 36 wherein the second plurality of power lands and the second plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the substrate.

38. (Previously Presented) The interposer recited in claim 36 wherein the capacitor comprises at least one high permittivity layer.

39. (Previously Presented) The interposer recited in claim 36 wherein the capacitor comprises a plurality of high permittivity layers.

40. (Previously Presented) The interposer recited in claim 39 wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second terminals, respectively.

41. (Canceled)

42. (Previously Presented) The interposer recited in claim 36, wherein the interposer comprises a multilayer ceramic structure.

43. (Previously Presented) The interposer recited in claim 36, wherein at least one of the power vias does not go entirely through the interposer.

44. (Previously Presented) The interposer recited in claim 36, wherein at least one of the ground vias does not go entirely through the interposer.

45. (Previously Presented) The interposer recited in claim 36, wherein the plurality of power and ground vias is a relatively large number.